PLEASE ENTER TLMD 01/29/2008

AMENDMENT

In the claims:

1 - 3. (Cancelled)

4. (previously presented) A pipeline accelerator, comprising:

a communication bus;

a plurality of pipeline units each coupled to the communication bus and each comprising a respective hardwired-pipeline circuit; and

wherein each of the hardwired-pipeline circuits is disposed on a respective field-programmable-gate–array die.

5 - 10. (Cancelled)

11. (previously presented) A computing machine, comprising:

a processor;

a pipeline-accelerator configuration registry operable to store hardwired-pipeline-configuration information;

a pipeline accelerator comprising,

a communication bus,

a pipeline-bus interface coupled to the communication bus, and

a plurality of pipeline units each coupled to the communication bus and each comprising a respective hardwired-pipeline circuit disposed on a respective field-programmable-gate–array die; and

a pipeline bus coupled to the processor, the registry, and the pipeline-bus interface of the pipeline accelerator, the pipeline bus operable to carry data between the processor and the pipeline accelerator and to carry the hardwired-pipeline-configuration information from the registry to the pipeline accelerator.

12. (original) The computing machine of clam 11 wherein:

the processor is operable to generate a message that identifies one of the pipeline units and to drive the message onto the pipeline bus;